REMARKS

Claims 1-12, and 13 are present in this application. Claim 11 has been canceled. Claim 1 is independent.

Drawings

Figure 21 has been objected to for not showing a legend such as "Prior Art." Applicants provide herewith a drawing correction showing the label "Prior Art," for Figure 21. Applicants request that the drawing objection be withdrawn.

Specification

The title has been objected to as not being descriptive. Applicants provide herewith a replacement title. Applicants request that the new title be entered.

Double Patenting

Claims 1-5 and 9-13 have been provisionally rejected on the ground of non-statutory obviousness-type double patenting over claims 1 and 8-13 of copending Application No. 10/506,322. Applicants will address the double patenting rejection in the event that all other issues have been resolved.

Claim Rejection under 35 USC 102(b) – Yoshikawa 1

Claims 1-5, 8, and 13 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,881,108 ("Yoshikawa 1"). Claim 1 has been amended. Applicants traverse the rejection based on the claims as amended.

According to the present specification as filed, at paragraph 0069,

> **[0069]** "The source/drain regions may be placed so as to overlap the edges of the gate electrode or may be placed so as to be offset relative to the edges of the gate electrode. In particular, in the case of being offset, the ease of inversion of the offset regions beneath the charge holding portions at the time of application of a voltage to the gate electrode varies greatly due to the amount of charge stored in the charge holding portions and, thereby, the memory effects are increased and the short channel effects are reduced, which is preferable. Here, in the case that the amount of offset is too great, a drive current between the source and drain is significantly reduced. Accordingly, the amount of offset should be determined so that the memory effects and the drive current both have appropriate values."

Present Fig. 1, for example, shows charge holding portions 61, 62 respectively overlapped with parts of the diffusion layer regions 17, 18.

These features are reflected in claim 1, which recites, among other things:

A semiconductor storage device comprising a semiconductor substrate, a gate insulating film, a single gate electrode, two charge holding portions, two diffusion layer regions, and a channel region. The charge holding portions "extend to an area above a portion of the channel region and overlap a portion of the respective diffusion layer regions such that the amount of current flowing between one of the diffusion layer regions and the other of the diffusion layer regions at the time of application of a voltage to the gate electrode is detected as being an indication of the

quantity of charge held in the first insulator, and the two diffusion layer regions are respectively offset relative to edges of the single gate electrode."

As can be seen in Fig. 1(b) of Yoshikawa 1, there is no overlap between the charge holding portions 108 and the diffusion layer regions 112, 113.

Thus, Applicants submit that Yoshikawa 1 fails to teach each and every claimed element of claim 1. Applicants request that the rejection be reconsidered and withdrawn.

Claim Rejection under 35 USC 102(b) – Sakagami

Claims 1-8 and 11-13 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,838,041 (Sakagami). Claim 1 has been amended. Applicants traverse the rejection based on the claims as amended.

Claim 1 requires that the two charge holding portions "extend to an area above a portion of the channel region and overlap a portion of the respective diffusion layer regions."

To the contrary, Sakagami teaches a charge holding portion 19 that is not formed on a portion of the channel region and does not overlap a portion of diffusion layer regions. Sakagami teaches a charge holding portion 19 formed entirely over a diffusion layer region(s).

Thus, Applicants submit that Sakagami fails to meet each and every claimed element, required by claim 1. Applicants request that the rejection be reconsidered and withdrawn.

Claim Rejection under 35 USC 102(b) – Yoshikawa 2

Claims 1-7 and 9-13 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,335,554 ("Yoshikawa 2"). Applicants traverse this rejection.

Claim 1 requires the claimed semiconductor storage device have "a single gate electrode."

To the contrary, Yoshikawa 2 teaches a semiconductor memory having two gate electrodes 3 and 8. Furthermore, gate electrodes 8 are formed on charge holding portions 4a and 4b.

The single gate electrode of the claimed invention is formed on the gate insulating film.

Thus, Applicants submit that Yoshikawa 2 fails to meet each and every claimed element, required by claim 1. Applicants request that the rejection be reconsidered and withdrawn.

Claim Rejection under 35 USC 102(e) – Kobayashi

Claims 1-10, 12, and 13 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Application 2003/0161192 (Kobayashi). Claim 1 has been amended. Applicants traverse the rejection based on the claim as amended.

Claim 1 requires "a single gate electrode" that is formed on the gate insulating film, and "two charge holding portions" "extended to an area above a portion of the channel region and overlap a portion of the respective diffusion layer regions."

To the contrary, Kobayashi teaches a nonvolatile semiconductor memory device including two electrodes comprised of a control gate electrode 5 and the memory gate electrode 7 (Kobayashi, Fig. 1A).

The difference in electrodes is because Kobayashi's nonvolatile semiconductor memory is directed to an entirely different structure than the present semiconductor memory. The present invention includes a single electrode connected as the word line. Unlike the present invention, Kobayashi discloses a memory gate electrode 7 as a word line, and the gate electrode 5 serving

as a the control gate (see Figs. 1A and 1B). In the present invention, the charge holding portion is formed only on side walls of the gate electrode. In Kobayashi, the charge storing film 6 is formed over the control gate 5, as well as in the entire region of the semiconductor substrate between control gates.

Thus, Applicants submit that Kobayashi fails to meet each and every claimed element, required by claim 1. Applicants request that the rejection be reconsidered and withdrawn.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should the Examiner have any questions regarding this matter, she is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), who may be reached in the Washington, DC, area at (703) 205-8000.

If necessary, the Commissioner is hereby authorized in this concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Dated: May 31, 2006

Respectfully submitted,

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